METHOD AND APPARATUS FOR AUTOMATIC ACTIVATION OF A CLOCK MASTER ON A STACKABLE REPEATER

ABSTRACT OF THE DISCLOSURE

An apparatus for automatically activating a clock master circuit in a stack of Fast Ethernet repeaters includes a first stackable Fast Ethernet repeater is disclosed. The first stackable Fast Ethernet repeater includes a first on pin having a first on pin logical state. The first on pin logical state is indicative of whether or not the first stackable Fast Ethernet repeater is configured in the stack of Fast Ethernet repeaters so that no other Fast Ethernet repeater occupying a position in the Fast Ethernet repeater stack that is before the position of the first Fast Ethernet repeater is powered on. A weak pull up voltage source is connected to the first on pin. The weak pull up voltage is derived from a switched power supply in the Fast Ethernet repeater so that when the Fast Ethernet repeater is powered on, the weak pull up voltage is present and when the Fast Ethernet repeater is powered off, the weak pull up voltage is not present. A clock master circuit has an enable input that is controlled by the first on pin logical state. A second stackable Fast Ethernet repeater includes a power state output pin. The power state output pin is configured to be connected to ground when the second Fast Ethernet repeater is powered on. A connector cable runs from the first Fast Ethernet repeater to the second Fast Ethernet repeater. The connector cable connects the first on pin from the first stackable Fast Ethernet Repeater to the power state output pin of the second stackable Fast Ethernet repeater. Thus, the clock master circuit in the first stackable Fast Ethernet Repeater is enabled based on whether the second stackable Fast Ethernet repeater is powered on.